Claims

- [c1] What is claimed is:
 - 1. A method of fabricating an integrated circuit, the integrated circuit having a semiconductor body, the method comprising following steps:
 - (a)forming a plurality of basic units on the semiconductor body, each of the basic units having an identical device characteristic; and
 - (b)forming at least a layout layer to program the basic units for generating a clocked logic circuit and a non-clocked logic circuit without placing restrictions on positions of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body.
- [c2] 2. The method of claim 1 wherein step (a) forms at least a transistor within each of the basic units.
- [c3] 3. The method of claim 2 wherein the transistor is an MOS transistor.
- [c4] 4. The method of claim 1 wherein step (b) utilizes the layout layer to program a basic unit for generating the clocked logic circuit.

- [05] 5. The method of claim 1 wherein step (b) utilizes the layout layer to program a plurality of basic units for generating the clocked logic circuit.
- [c6] 6. The method of claim 1 wherein step (b) utilizes the layout layer to program a basic unit for generating the non-clocked logic circuit.
- [c7] 7. The method of claim 1 wherein step (b) utilizes the layout layer to program a plurality of basic units for generating the non-clocked logic circuit.
- [08] 8. The method of claim 1 wherein step (a) forms at least a PMOS transistor and at least an NMOS transistor within each of the basic units.
- [09] 9. A method of fabricating an integrated circuit, the integrated circuit having a semiconductor body, the method comprising following steps:

 (a)forming a plurality of basic units on the semiconductor body, each of the basic units having a plurality of first transistors cascaded in a series and a plurality of second transistors cascaded in a series; and

 (b)forming at least a layout layer to program traces among the first transistors and the second transistors of at least a basic unit for controlling the basic unit to form either a clocked logic circuit or a non-clocked logic cir-

cuit.

- [c10] 10. The method of claim 9 wherein the first transistors are not electrically connected to the second transistors before the traces are programmed.
- [c11] 11. The method of claim 9 wherein the first transistors and the second transistors are MOS transistors.
- [c12] 12. The method of claim 11 wherein the first transistors are PMOS transistors, and the second transistors are NMOS transistors.
- [c13] 13. The method of claim 9 wherein step (b) utilizes the layout layer to program the basic units for generating the clocked logic circuit.
- [c14] 14. The method of claim 9 wherein step (b) utilizes the layout layer to program the basic units for generating the non-clocked logic circuit.
- [c15] 15. An integrated circuit comprising:
 a semiconductor body for positioning a plurality of basic unit, each of the basic units having an identical device characteristic;
 a clocked logic circuit formed on the semiconductor body, the clocked logic circuit being formed by at least a basic unit; and

a non-clocked logic circuit formed on the semiconductor body, the non-clocked logic circuit being formed by at least a basic unit;

wherein the semiconductor body does not limit locations of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body.

- [c16] 16. The integrated circuit of claim 15 wherein each of the basic units comprises at least a transistor.
- [c17] 17. The integrated circuit of claim 16 wherein the transistor is a MOS transistor.
- [c18] 18. The integrated circuit of claim 15 wherein each of the basic units comprises at lease a PMOS transistor and at least an NMOS transistor.
- [c19] 19. An integrated circuit comprising:
 a semiconductor body for positioning a plurality of basic
 units, each of the basic units having a plurality of first
 transistors cascaded in a series and a plurality of second
 transistors cascaded in a series;
 - a clocked logic circuit formed on the semiconductor body, the clocked logic circuit being formed by at least a basic unit; and
 - a non-clocked logic circuit formed on the semiconductor, the non-clocked logic circuit being formed by at

least a basic unit.

- [c20] 20. The integrated circuit of claim 19 wherein the first transistors are not electrically connected to the second transistors.
- [c21] 21. The integrated circuit of claim 19 wherein the first transistors and the second transistors are MOS transistors.
- [c22] 22. The integrated circuit of claim 21 wherein the first transistors are PMOS transistors, and the second transistors are NMOS transistors.